Development of an Ultra-high Density Power Chip on Bus (PCoB) Module

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Abstract—A traditional power module uses metal clad ceramic (e.g. DBC or DBA) bonded to a baseplate that creates a highly thermally resistive path, and wire bond interconnect that introduces substantial inductance and limits thermal management to single-sided cooling. This paper introduces a Power Chip on Bus (PCoB) power module approach that reduces parasitic inductance through an integrated power interconnect structure. The PCoB maximizes thermal performance by direct attaching power chips to the busbar, integrating the heatsink and busbar as one, and uses a dielectric fluid, such as air, for electrical isolation. This new power module topology features all planar interconnects and double-sided air cooling. Performance evaluations are carried out through comprehensive electrical and multi-physics simulation and thermal testing for a 1200V, 100A rated single-switch PCoB design. Fabrication and assembly processes are included. For the developed double-sided air-cooled module, 0.5°C/W thermal resistance and 8nH power loop parasitic inductance are achieved.

Keywords—double-sided power module; air cool; all planar interconnection; low inductance

I. INTRODUCTION

With the commercialization of wide-bandgap (WBG) power semiconductor devices, the traditional power package has reached its limit to take advantage of WBG performance both electrically and thermally. Electrical and thermal limitations due to ceramics, thermal interface material (TIM), flexible welded interconnects (e.g. wire bonds) and use of single-sided cooling is well documented [1, 2]. The widely used direct bonded copper (DBC) substrate accounts for significant portion of junction to case thermal resistance. The bond wire can introduce significant amounts of inductance that may introduce harmful power device switching transients. To increase electrical and thermal performance, planar interconnects and double-sided cooling have become key areas for development. In late 1990’s, GE developed the Power Overlay (POL) package [3]. In 2008, Denso manufactured the double-sided power module for the Lexus LS600h hybrid car power conversion unit [4]. In the past few years, both industry and academia show a growing interest in double-sided power module development [5-15].

Elevated temperature within a power module during dissipation introduces mechanical stresses in both the power device and package due to difference in coefficients of thermal expansion (CTE) of materials. The accumulated stress in each layer may reduce reliability and cause power module mechanical failure. Moreover, due to its brittle nature, high stresses induced in the power semiconductor materials could result in detrimental fracturing in the die [16]. The thermal stress issue is more challenging for double-sided power modules than the standard single-sided DBC substrate based power modules, when dies are sandwiched by interconnect metal traces on both sides. This is especially an issue for high current modules with double-sided thick copper interconnects and large die area. Additionally, package fabrication and assembly are more complicated with the need for non-standard top-side solderable die, sophisticated top side interconnect alignment process and top-to-bottom voltage isolation.

This paper proposes a double-sided air-cooled Power Chip on Bus (PCoB) module design featuring liquid-cooled equivalent thermal performance, ultra-low electrical parasitics and robust thermal-mechanical stress management. The proposed PCoB structure has a basic topology as shown in Fig. 1. Thick finned copper acts as both heatsink and busbar. Power dies are electrically attached to 2 busbar-like power substrates directly. Molybdenum spacers are used as CTE buffer between die and bottom substrate for reducing thermal-mechanical stress caused by CTE mismatch. The thickness of molybdenum spacer is optimized through thermal-mechanical finite element analysis (FEA) simulation. Bottom-side die attachment for MOSFET drain and diode cathode is through soldering. Upper die attachment is through silver loaded silicone for further thermal-mechanical stress reduction. The gate terminal is connected with
polyimide flexible circuit. Electrical isolation between the electrically hot heat sinks to the environment is achieved through an air channel.

II. DESIGN OF SINGLE SWITCH PCoB MODULE

A. Single switch PCoB module topology

The single switch version of PCoB module includes an active switch and an anti-parallel diode. The module is designed for 1200V and 100A. Two Wolfspeed 1200V, 50A SiC MOSFETs (CPM2-1200-0025B) and 1 Wolfspeed 1200V 50A anti-parallel SiC Schottky diode (CPW5-1200-Z050B) bare dies are chosen for each module.

The designed single switch module with its integrated heatsinks has a dimension of 41 by 41 by 43 mm³ and weight of 65 grams. The gate pads of MOSFETs are connected through an integrated 2-layer flexible circuit with 1 oz. copper each layer. This flexible circuit also compensates the thickness difference between the chosen diode and MOSFET bare dies. The flexible circuit layout includes Kelvin connection for the source of MOSFETs. The gate and source traces are placed with maximized overlap area to reduce gate loop inductance.

B. Parasitic extraction of single switch PCoB

Electrical parasitics are extracted through ANSYS Q3D extractor. In order to compare with regular power module, a non-destructive method is proposed to accurately measure the internal dimensions of regular power module and a 3D model of regular SiC six pack module (Wolfspeed CCS050M12CM2) is generated for parasitics comparison [2]. Both power loop and gate loop parasitic inductances are simulated for PCoB module and regular SiC six pack module. The simulation also indicates the current density distribution of the current path of concern. As summarized in the following table, PCoB module features lower parasitic inductance for both power loop and gate loop. The reduction of gate loop inductance will reduce the gate driver signal ringing and decrease the required external gate resistor value. The switching will be faster and the switching loss will be smaller. Additionally, the reduced power loop inductance will lead to less di/dt induced voltage spike across the switch. Due to the geometric compactness of PCoB, the half bridge version module will have a similar power loop inductance.

<table>
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<th>Power loop inductance (nH) @ DC</th>
<th>Gate loop inductance (nH) @ DC</th>
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<tr>
<td>CCS050M12CM2</td>
<td>35</td>
<td>25</td>
</tr>
<tr>
<td>PCoB module</td>
<td>8</td>
<td>4</td>
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C. Voltage blocking test

The PCoB module integrates two busbar-like substrates attached to the source and drain pads of the MOSFET dies. These two substrates have been bonded together through a preformed epoxy. The chosen epoxy has a curing temperature of 150°C for 40 minutes and an operation temperature up to 204°C. A test PCoB structure without power die has been made to test the voltage blocking capability with the chosen epoxy bonding material. The tested module withstands 2000V easily. Another diode only module has been tested for reverse leakage at 25°C. The leakage current is well within the bare die diode’s datasheet. The module under test blocks 1300V for less than 200µA.
D. Thermal performance evaluation

Temperature increase due to power semiconductor heat dissipation affects the device performance and reliability significantly [17]. Detailed 3D CAD model has been created in Solidworks for air-cooled thermal FEA simulation. COMSOL Multi-physics software is chosen. Heat transfer and laminar flow physics are coupled in this case. Heat transfer in both solid and fluid is included. The FEA model has a mesh of 539158 elements with average element quality above 0.7 for achieving a reasonable simulation accuracy. In the model, the ambient temperature is fixed at 20°C, 100w power dissipation is assigned to one SiC power die and various air flow rates are simulated. In order to study the impact of different die size, both 5×5 mm² and 10×10 mm² dies are studied. The junction to ambient thermal resistance is calculated by maximum die temperature minus ambient temperature then divided by power dissipation. The simulated junction to ambient thermal resistances are summarized in table below. For this PCoB design, since the junction to case thermal resistance is only a fraction of junction to ambient thermal resistance, the die size has very small influence to the overall junction to ambient thermal resistance. Based on the thermal resistance of 10×10 mm² die under 30 CFM air flow rate, the power dissipation capability is summarized in Fig.9. The designed single switch PCoB platform is able to dissipate 122w for maximum junction temperature of 150°C and ambient temperature of 100°C.

<table>
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<th>Table II. Simulated Thermal Resistance</th>
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<tr>
<td>Air flow rate (CFM)</td>
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<td>( R_{th,ja} ) for 5×5 mm² die (°C/w)</td>
</tr>
<tr>
<td>( R_{th,ja} ) for 10×10 mm² die (°C/w)</td>
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A diode only version was first fabricated to test thermal dissipation performance. The tested module utilize a Wolfspeed (CREE) CPW5-1200-050B 1200V, 50A silicon carbide Schottky diode chip with the chip size about 5mm by 5mm. Previous simulation indicates the maximum junction temperature is approximately within 2 °C difference from the maximum substrate temperature. Thus the measured maximum substrate temperature is used to estimate the junction to ambient thermal resistance. The thermal test indicates 0.5°C/W junction to ambient thermal resistance at air flow rate of about 15 CFM. And the thermal resistance without any active cooling is less than 5°C/W. Fig.10. shows the infrared temperature image for 15w dissipation without any active cooling.

For similar die size, the traditional power module with 25 mil AlN substrate and 12 mils copper on Ni plated baseplate gives about 0.4°C/W junction to case thermal resistance. Putting the module on a liquid-cooled cold plate through thermal grease interface the total junction to liquid thermal resistance is about 0.6–1.0 °C/w. The double-sided air cooled PCoB module features enhanced thermal performance.
E. Thermal-mechanical stress management

Due to the CTE mismatch, thermal-mechanical stress management is critical for any high current double-sided power module. To reduce the thermal-mechanical stress, two approaches are taken in PCoB power module. Molybdenum spacers with low CTE is used as a mechanical buffer layer soldered between power die and substrate. An FEA simulation indicates the influence of thickness of molybdenum spacer to die maximum stress. Customized gold plated molybdenum spacer with a thickness of 0.75mm is fabricated for this project. Upper die attachment is achieved by silver loaded silicone for further thermal-mechanical stress reduction. FEA simulations indicate the silver loaded silicone reduces the maximum Von Mises stress of the chip from 11.5 MPa to 6.63 MPa, a 40 percent decrease compared to double-sided tin-lead soldering. The chosen silver loaded silicone material has properties as shown in the table below.

III. POWER SEMICONDUCTOR TOP SIDE METALIZATION

Regular power die has an aluminum top side metallization for wire bonding. In order to have a compatible top side metal for double-sided all planar interconnect, a fabrication process is developed for customizing power die top metal in our on campus clean room. Most semiconductor process equipment is designed for processing the whole wafer. In order to have the flexibility to utilize small number of commercial dies from different manufacturers, a special effort has been made to develop a process on die level. In this work, E-beam deposition of titanium, nickel and silver for 300 nm, 300 nm, 1000 nm respectively is achieved with good solderability. Fig.12. shows the E-beam deposition system.

A. SiC schottky diode top side metallization

Wolfspeed (CREE) CPM2-1200-0025B 1200V, 50A silicon carbide power MOSFET is chosen for the PCoB power module. The die size is 6.44 mm by 4.04 mm. The original top side metal is Al and the back side is Ni/Ag. Due to the relatively small feature size near gate area, photo-resist with mask aligner approach is taken. In order to reduce the possibility of gate to source short during PCoB assembly process, the designed photo mask leaves larger distance from gate to source. The complete process includes: 1) Die cleaning, 2) Photoresist spinning, 3) Bake, 4) Photo mask alignment and UV exposure, 5) Bake, 6) Photoresist develop, 7) Plasma etch, 8) Alumina etch, 9) E-beam deposition for Ti/Ni/Ag, 10) Liftoff. The device handling, photoresist spinning profile, UV exposure time, photoresist development time and liftoff time have all been tuned for the specific die. Details of the process steps and results are provided to assist the reader in reproducing the process.

In Fig. 15. A) the light yellow part is photoresist, the light silver and gray areas are the original metal pads on MOSFETs. In Fig. 15. B) the newly deposited metal can be seen clearly in contrast with the original metal. Due to the height difference between the original gate pad and source pad, they looked different even with same metallization.
C. Test

Solderability test has been done on different samples. The original top side metal is aluminum which is non-solderable. When soldering the original die, the solder forms a sphere and there is no wetting on top metal pad. When soldering the deposited SiC die with excess amount of eutectic Sn63/Pb37 solder paste, the solder wets very well to the deposited area. Self-alignment prevent the gate to source short. The brown mark near the wetted area in Fig.16, B, C) is solder flux. Overall, the deposition pattern is well controlled and the solder wets easily.

To test the current conduction through the new metal deposition, a DBC substrate based test bed has been fabricated as in Fig.17. The original diode die top side is connected though bondwire, deposited dies are connected by soldering the copper strip to the top side.

The test module has been measured by Tektronix 371B high power curve tracer with kelvin connection. For forward conduction up to 100A, the deposited die behaves almost identical to the original die.

IV. POWER CHIP ON BUS (PCoB) MODULE ASSEMBLY

The assembly flow is summarized in the following chart.

A. Machining and plating

Ideally, the substrates and heatsinks can be made as one piece for reducing the additional interface. Due to the complexity for machining, heatsinks and substrates are made separately and soldered together for fast prototyping. The wire EDM has been used for the fabrication of copper heatsinks. Copper substrates have been fabricated with CNC machining. After the machining, the heatsinks and substrates are electrically plated with nickel for surface protection.

B. Soldering

A 5-zone reflow oven is used to solder the heatsinks to substrate, gold plated molybdenum spacer to substrate and die to molybdenum spacer. The Sn10/Pb88/Ag2 solder is chosen as high temperature solder for heatsink soldering. The Sn63/Pb37 solder is used for molybdenum soldering and die attachment.
C. Cast molding and curing

A high resolution 3D printed mold is designed and fabricated for forming the silicone mold for PCoB module encapsulation. The chosen epoxy underfill material features low coefficient of thermal expansion under glass transition temperature of 145 ℃.

<table>
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<tr>
<th>TABLE IV. ENCAPSULATION MATERIAL PROPERTIES</th>
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<tr>
<td>Dielectric strength</td>
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<tr>
<td>500 V/mil @AC</td>
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<tr>
<td>Cure time</td>
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</table>

Fig. 22. Reflow soldering

ANSYS Q3D simulation indicates that the power loop parasitic inductance across each phase leg (with small difference between center phase leg and outside phase leg) is less than 10nH which is only 1/3 of Wolfspeed 1200V 50A six pack module. Thermal FEA simulation indicates a junction to ambient thermal resistance of 0.52 to 0.75 C/W (depending on die location) at air flow rate of 30CFM. Hence, air cooling is a viable alternative to liquid cooled traditional approaches in EV/HEV application.

VI. CONCLUSIONS

The paper validates the viability of a double-sided air cooled Power Chip on Bus (PCoB) module versus regular liquid cooled. Extensive multi-physics simulation and verification show less than 10nH power loop and less than 5nH gate loop parasitic inductances. About 0.5 ℃/W junction-to-ambient thermal resistance is achieved by air cool. Also a 260˚C die attachment material is introduced along with a process to create double-sided die attachment. 2000V blocking capability is verified through experiment for the proposed package structure. The PCoB design is extended to a 35kW EV motor drive that uses an integrated boost stage plus three phase VSI in the module. The next step of research for PCoB includes switching test and multiple-switch PCoB module fabrication and implementation.

ACKNOWLEDGMENT

This work was performed at NCSU Packaging Research in Electronic Energy Systems (PREES) Lab.
The information, data, or work presented herein was funded in part by the Office of Energy Efficiency and Renewable Energy (EERE), U.S. Department of Energy, under Award Number DE-EE0006521 with North Carolina State University, PowerAmerica Institute

This work was performed in part at the NCSU Nanofabrication Facility (NNF), a member of the North Carolina Research Triangle Nanotechnology Network (RTNN), which is supported by the National Science Foundation (Grant ECCS-1542015) as part of the National Nanotechnology Coordinated Infrastructure (NNCI).

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