PowerAmerica

Annual Meeting

North Carolina State University
Dr. Veena Misra

January 17 – 19, 2017

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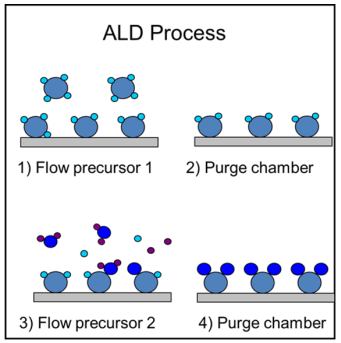
Misra Group at NCSU

- **Over 9 years experience in wide band gap research on SiC, GaN and Ga_2O_3. World leaders in atomic layer deposited (ALD) dielectrics for enhancing power device, logic, memory and sensor applications.**

- **SiC device research in PowerAmerica Device Development track**



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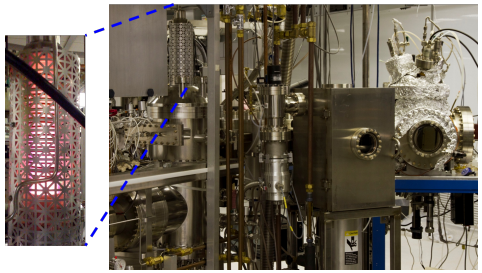
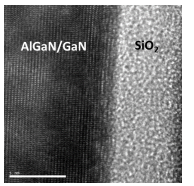
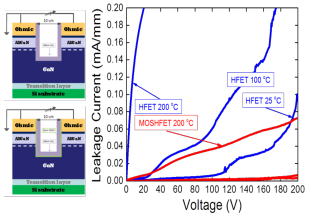
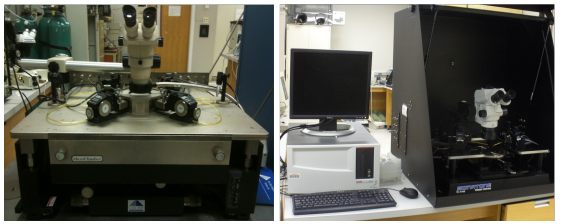


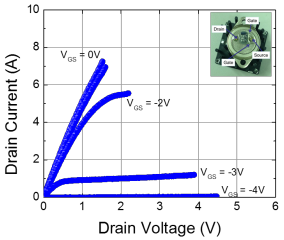
Capabilities:
Si and III-V transistor devices
FG and Resistance memory devices
GaN and SiC power devices
Magnetic devices
Bio-FET and solar cells

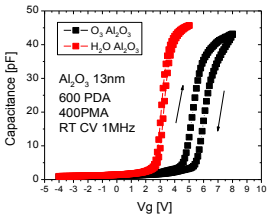
Equipment:
4 probe stations
3 IV meters, 2 CV meters
3 pulse generators, 2 Oscilloscopes
2 Temperature controlled chucks











FREEDM systems center

SSIST

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Project Objectives

- **The primary objectives are to:**
  - Demonstrate high mobility SiC MOSFETs based on incorporation of rare earth and high-k dielectrics using a manufacturable process flow for medium voltage (<1700V) power switch device application

- **Key Performance measures:**
  - Reliability, mobility, threshold voltage and high temperature performance

- **Broader impact on the WBG community:**
  - Our novel approach for SiC research provides 1) a fabrication cost reduction by achieving high mobility and 2) better gate stack reliability by process optimization and innovation.

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Milestones and Deliverables

- **Open foundry process & stability / reliability assessment**
  - Fabricate SiC MOSFET with ALD dielectric on foundry wafer (Month 12)
  - V_T shift < 0.4V under ± 4MV/cm stress at RT (Month 4)
  - V_T shift < 0.5V under ± 4MV/cm stress at 150°C (Month 7)
  - TDDB and MTTF evaluation at RT (Month 7)
  - V_T shift < 0.5V under ± 4MV/cm stress at 150°C (Month 12)

- **Optimizing gate stacks for mobility**
  - ALD SiO_2 and rare earth dielectric: V_T shift < 0.5V under ± 4MV/cm at RT (Month 6)
  - ALD SiO_2 and rare earth dielectric: V_T shift < 0.5V under ± 4MV/cm at 150°C (Month 12)
  - Lateral MOSFET with V_T > 3V and mobility > 100 $cm^2/V{\cdot}s$ (Month 9)

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Monthly progress and quarterly milestones

Task	Task/Subtask description	Milestone	Q1			Q2			Q3			Q4		
			1	2	3	4	5	6	7	8	9	10	11	12
Task 1. Open foundry process & stability/reliability assessment														
1.1	Fabricate SiC DMOSFET with ALD dielectric on foundry wafer	Mobility > 50 $cm^2/V{\cdot}s$, V_T shift < 0.5V												
1.2	V_T instability of in house lateral MOSFET	V_T shift < 0.4V under ±4MV/cm (RT)												
	V_T instability of in house lateral MOSFET	V_T shift < 0.5V under ±4MV/cm (150°C)												
1.3	V_T instability of MOSFET from foundry	V_T shift < 0.4V under ±4MV/cm (RT)												
	V_T instability of MOSFET from foundry	V_T shift < 0.5V under ±4MV/cm (150°C)												
1.4	Long-term integrity/Reliability evaluation	TDDB and MTTF evaluation of ALD oxides (RT)												
	Long-term integrity/Reliability evaluation	TDDB and MTTF evaluation of ALD oxides (150°C)												
Task 2. Optimizing gate stacks for mobility > 100 $cm^2/V{\cdot}s$														
2.1	Growth condition optimization	Mobility and V_T vs. thickness trade-off												
2.2	Process parameter optimization	V_T > 3V and Mobility > 100 $cm^2/V{\cdot}s$												
2.3	V_T instability of MOSFET with rare-earth oxide/ALD SiO_2	V_T shift < 0.5V under ±4MV/cm (RT)												
	V_T instability of MOSFET with rare-earth oxide/ALD SiO_2	V_T shift < 0.5V under ±4MV/cm (150°C)												

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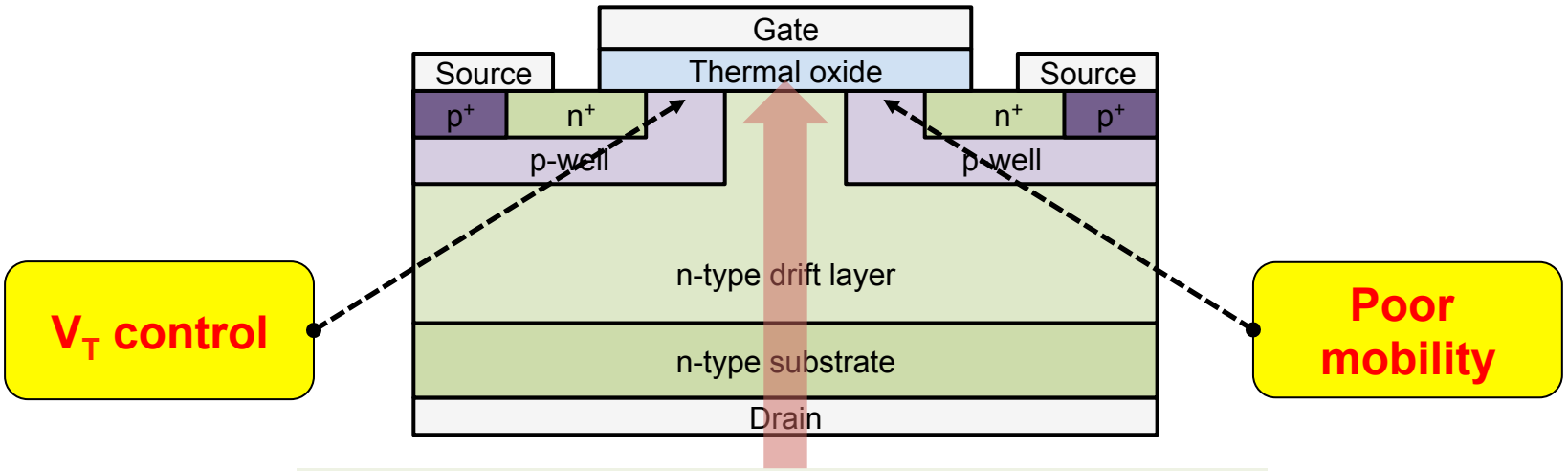
SiC R&D: Introduction and Approach

Current issues of SiC MOSFET



High interface states density (D_{it})
- **Carbon rich interfacial layer**
- **Clustered carbons**
- **Dangling bonds**

- **Poor mobility**
- **Mobility / Threshold voltage (V_T) trade-off**

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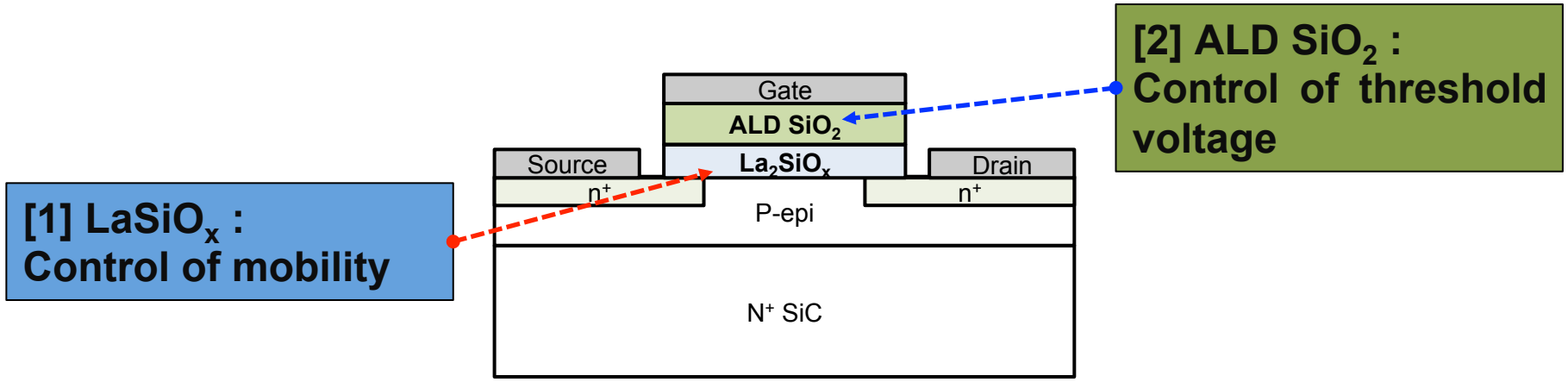
SiC R&D: Introduction and Approach

Approach



[1] Advantages of $LaSiO_x$

- Scavenging effect[1,2]
- Resistant to crystallization up to 900°C[1]

[2] Using ALD SiO_2 on SiC

- No substrate oxidation
- Precise thickness control
- Ideal for trench MOSFETs
- Negative charge

1. J. -P. Maria et al., J. Appl. Phys., Vol. 90, No. 7, 2001.
2. 2. H. Iwai et al., IEDM Tech. Dig., pp.625-628, 2002.

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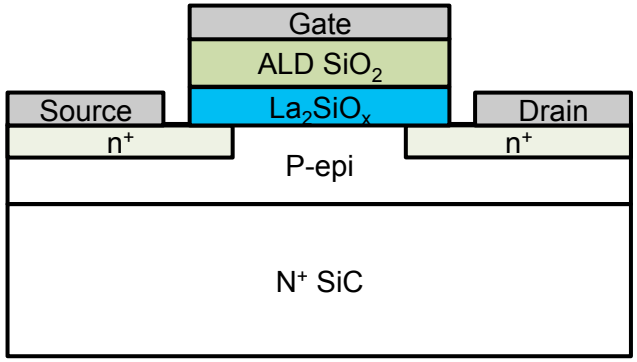
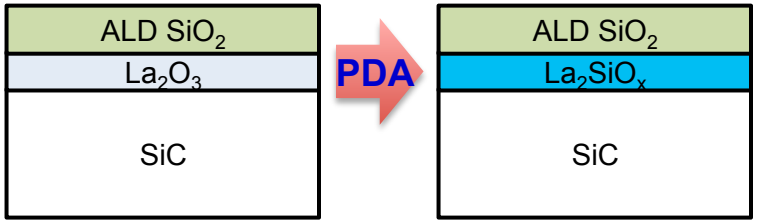
SiC MOSFET with La_2O_3/ALD SiO_2 fabrication

- S/D implantation and activation
- La_2O_3 deposition using a MBE tool
- 30nm ALD SiO_2 deposition at 150°C substrate temperature
- Post deposition anneal (PDA) in N_2O at 900°C
- Gate electrode deposition
- Contact hole etching
- S/D Nickel deposition
- S/D silicide formation anneal at 950°C

Lateral MOSFET





4H-SiC, Si-face, 8° off axis, p-type epi-layer doping 5E15cm^{-3}

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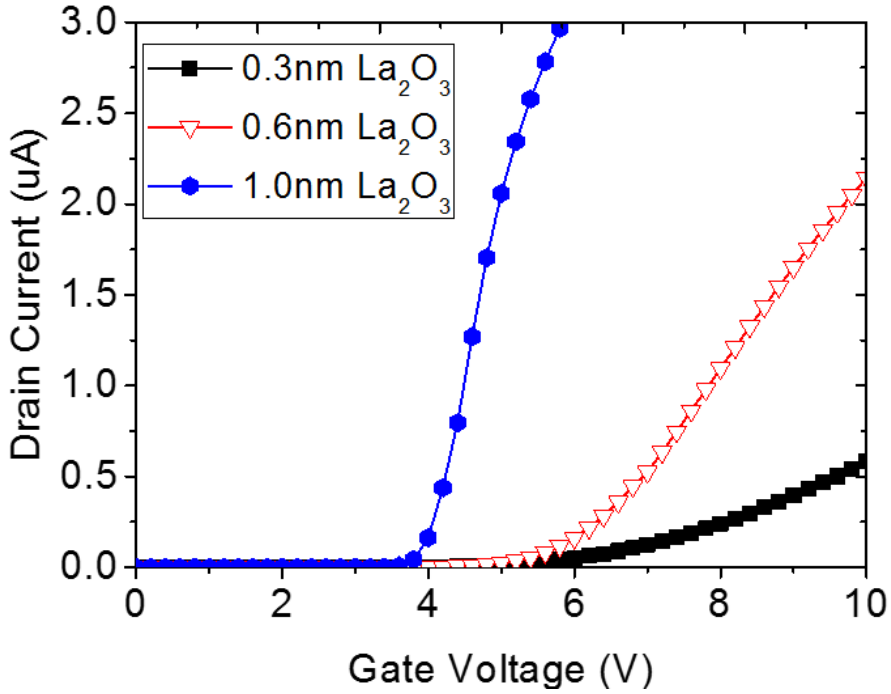
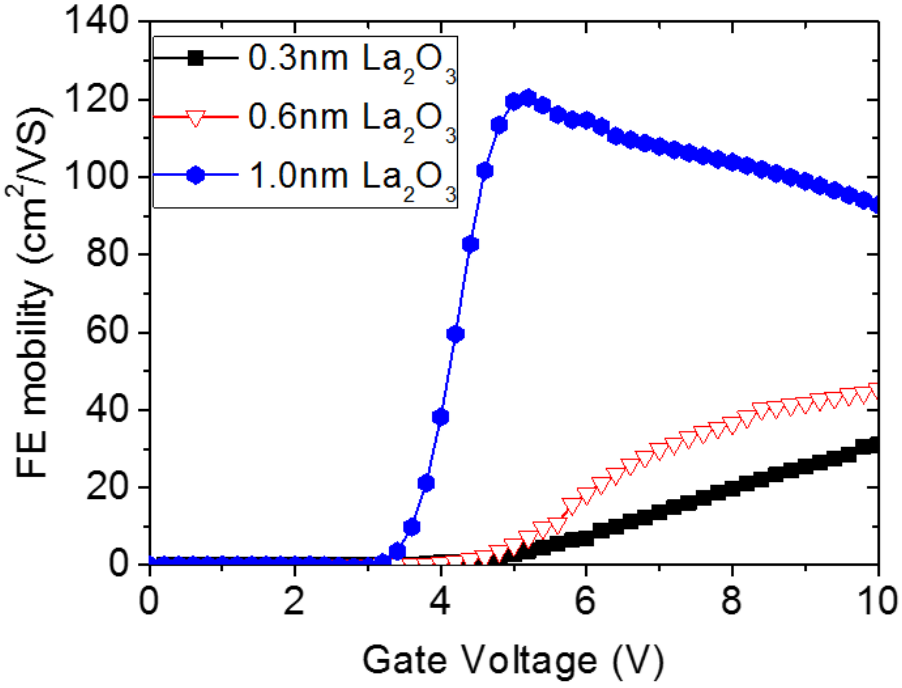
SiC MOSFET with La_2O_3/ALD SiO_2

$I_{DS} – V_{GS}$ Characteristic



Field Effect Mobility



- **High mobility and positive threshold are achieved with LaO/SiO_2 dielectric**
- **Lateral MOSFET with La_2O_3 give the higher mobility > 120cm^2/V·s**

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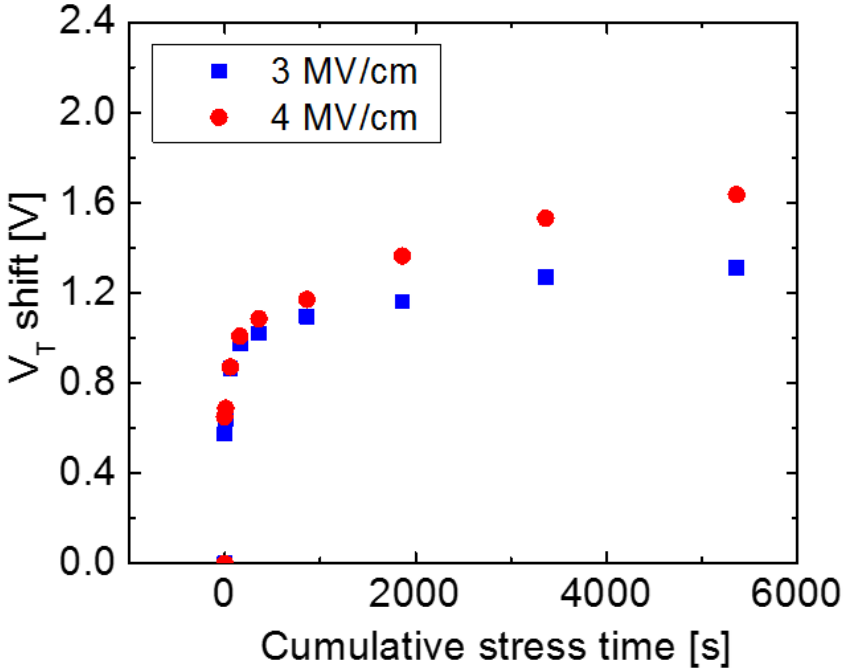
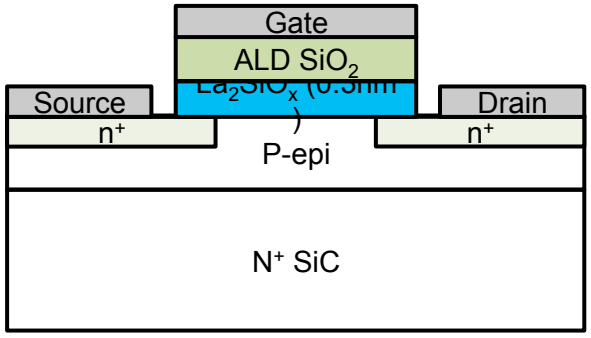
Reliability results (in BP1)

PBTI Test at RT





- MOSFET with 0.3nm La_2O_3/ALD SiO_2
  - V_T shift ~ 1.6V under 4MV/cm stress
  - Electron trapping in La-silicate
    → Need process optimization

Our Approach

High temperature Rapid Thermal Annealing Forming Gas Anneal (RTA-FGA) to improve $LaSiO_x$ layer

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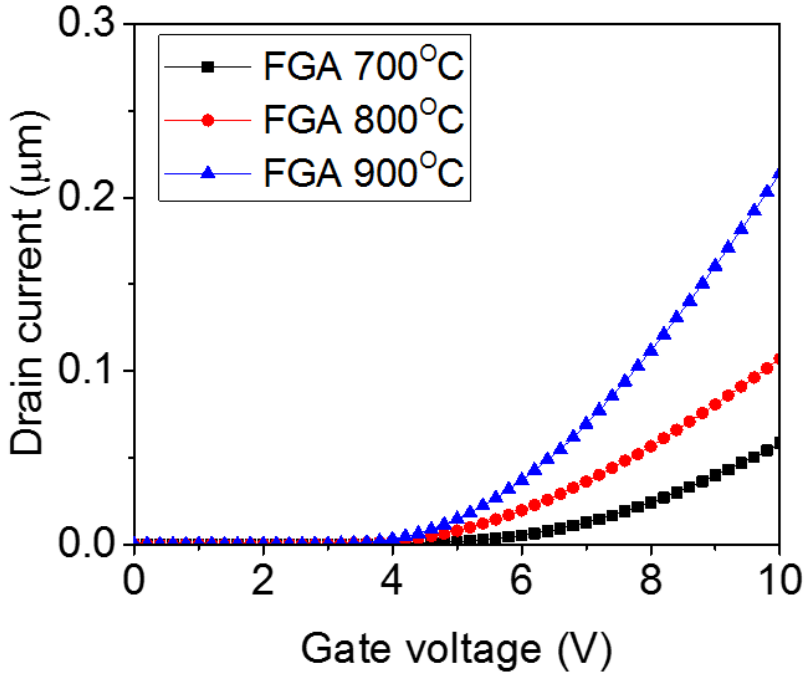
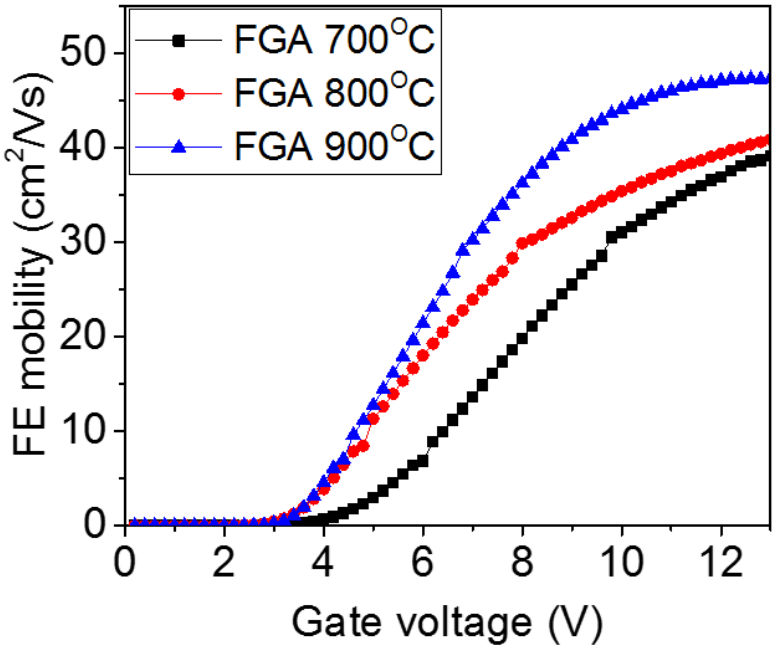
La_2O_3 0.3nm/ALD SiO_2 MOSFET : FGA effect

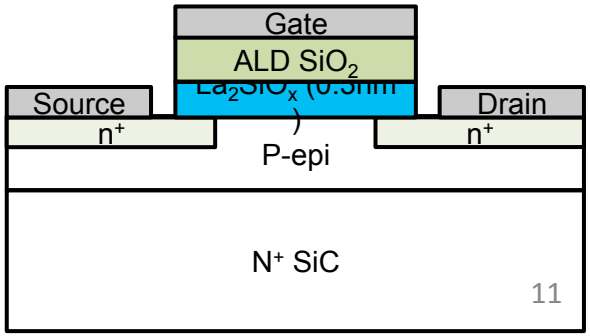
Transfer characteristic



Field-effect Mobility



- **La_2O_3 0.3nm/ALD SiO_2 : FGA reduces the V_T and the improved mobility**



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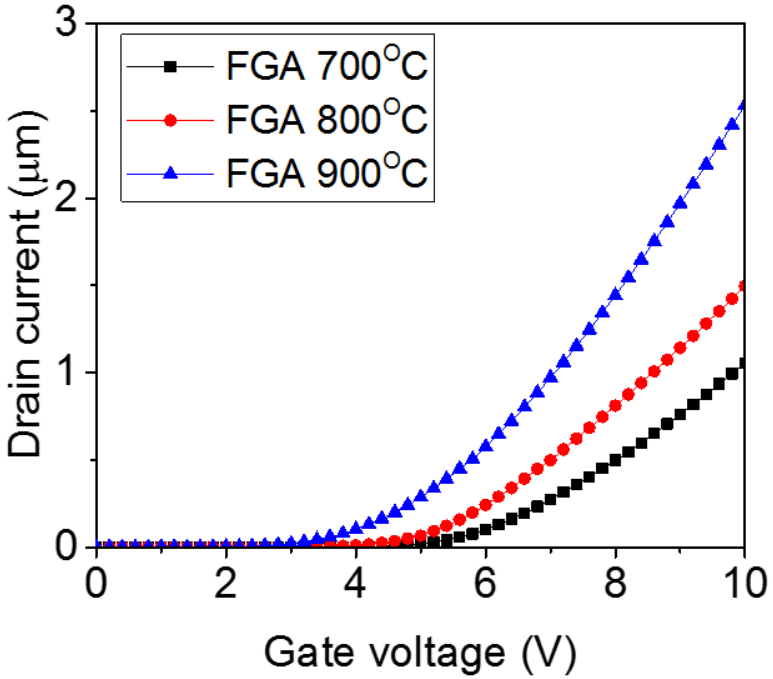
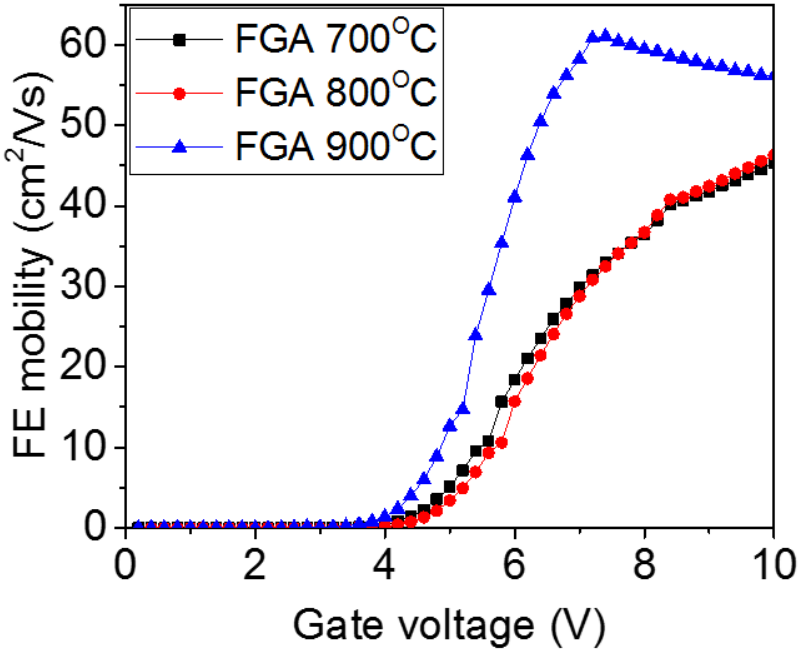
La_2O_3 0.6nm/ALD SiO_2 MOSFET : FGA effect

Transfer characteristic



Field-effect Mobility



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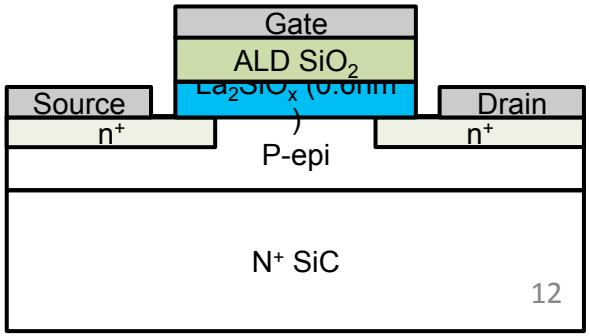

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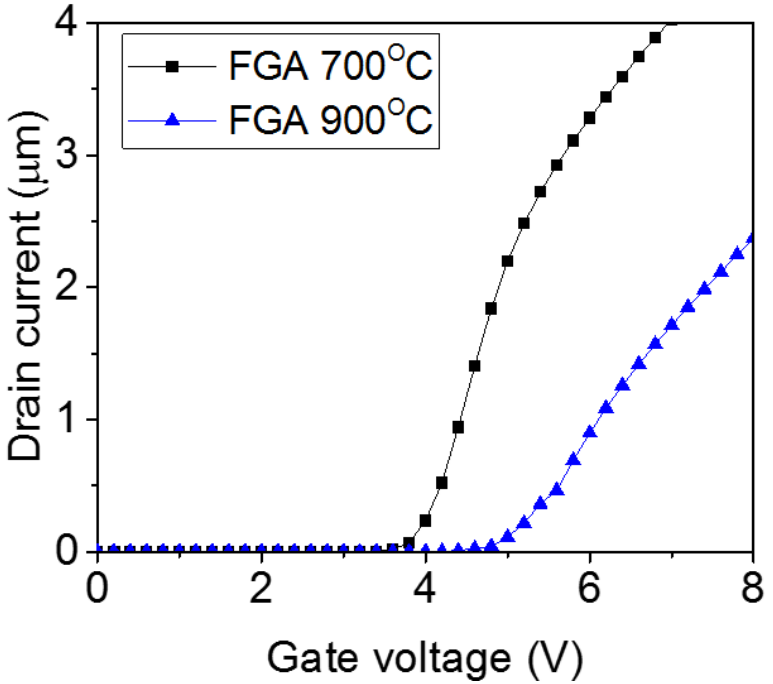
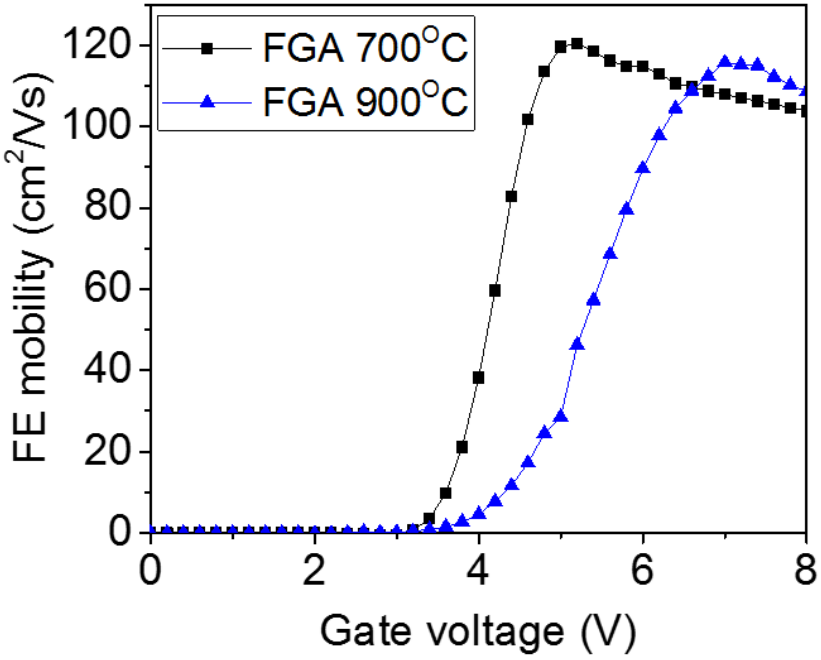
La_2O_3 1.0nm/ALD SiO_2 MOSFET : FGA effect

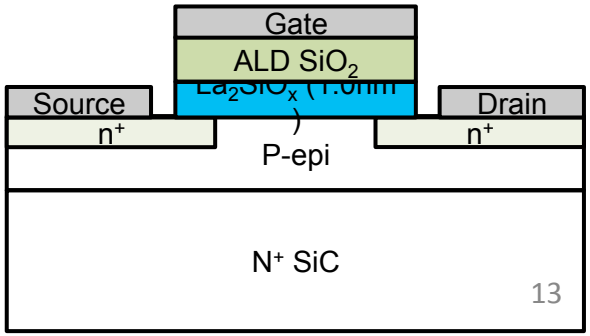
Transfer characteristic



Field-effect Mobility



- **La_2O_3 1.0nm/ALD SiO_2 : FGA not affect the V_T and the mobility**



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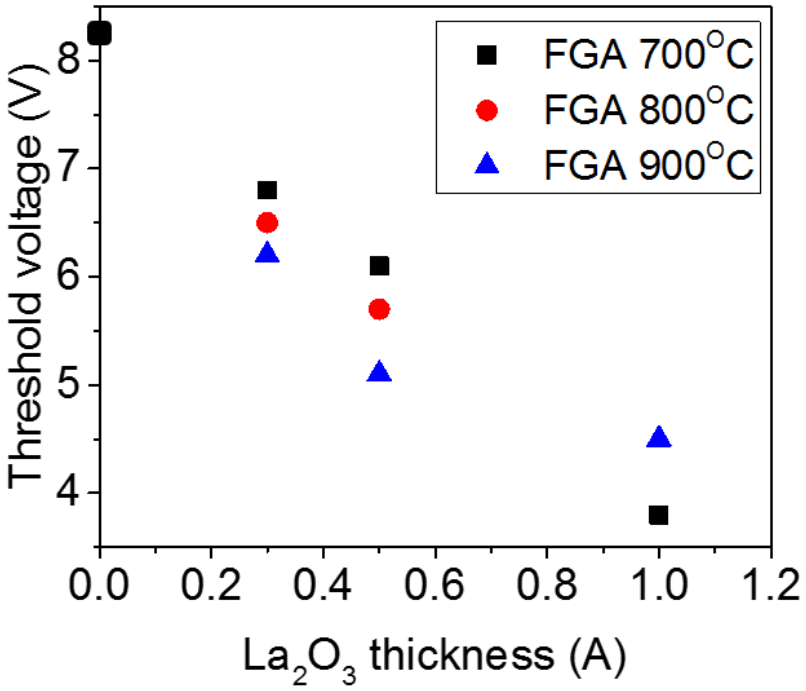
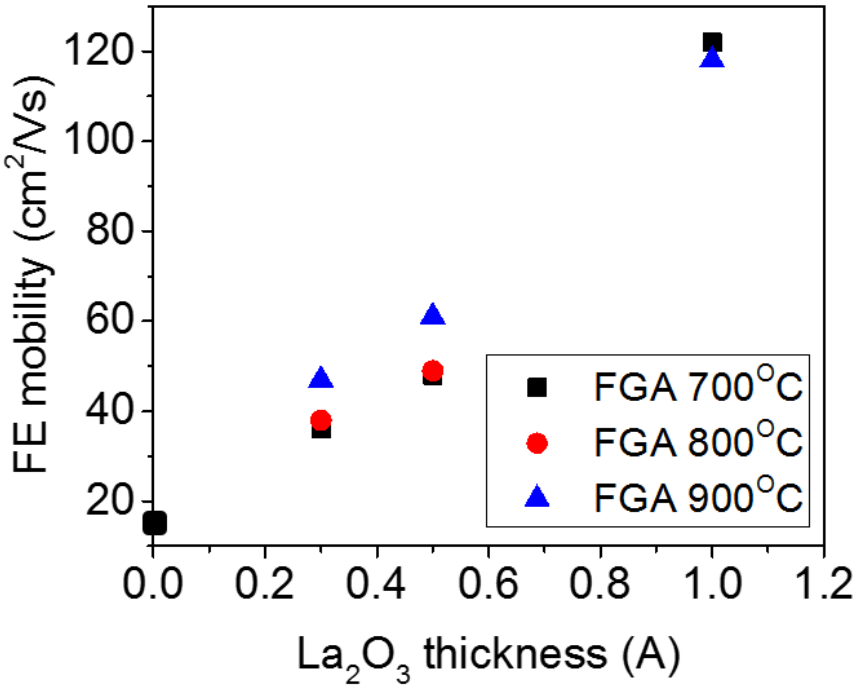
Summary of V_T and mobility (After FGA)

V_T vs. La_2O_3 thickness



Mobility vs. La_2O_3 thickness



- **By inserting a $LaSiO_x$ layer at SiC/SiO_2**
  - ➔ **Interface properties have been significantly improved**
  - ➔ **1nm La_2O_3 : V_T > 3 V and mobility > 120$cm^2/V{\cdot}s$**
- **Below 0.5nm La_2O_3 : FGA improve the V_T and the mobility**

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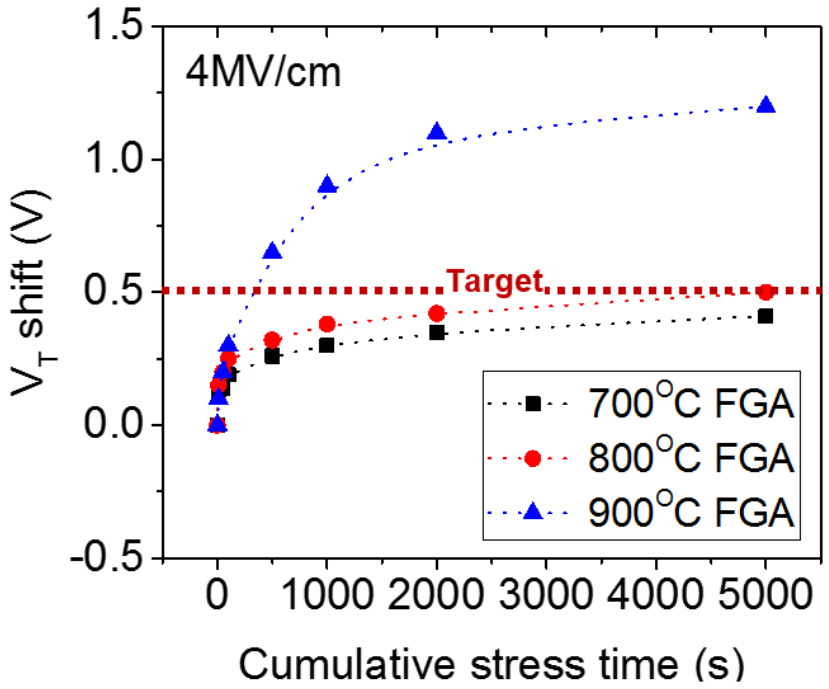
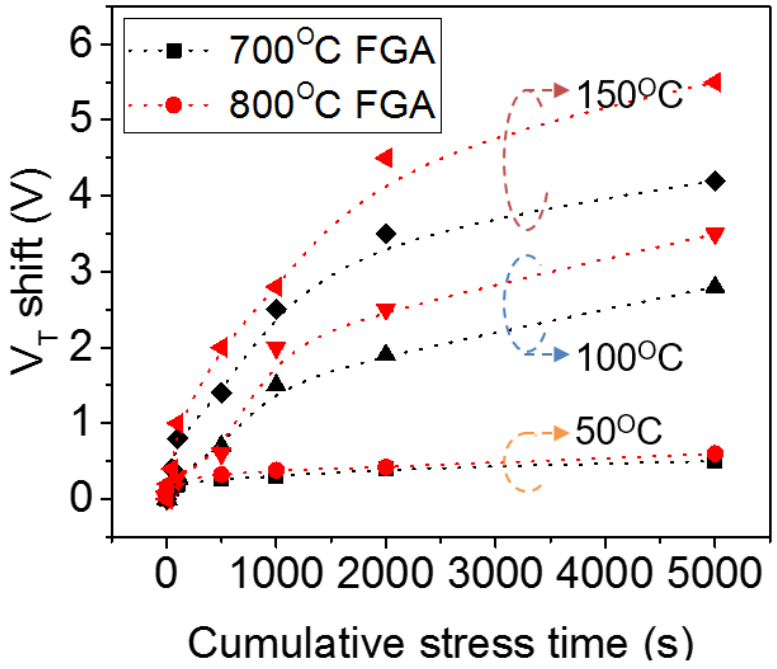
Optimization for better reliability : FGA Effect

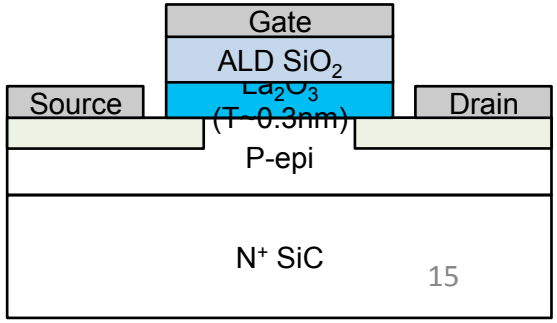
PBTI Test at RT



PBTI @ high temperature



- **700°C and 800°C FGA give the best V_T stability**
  - **<0.5V under 4MV/cm stress**
- **V_T shift significantly increases at high temperature**



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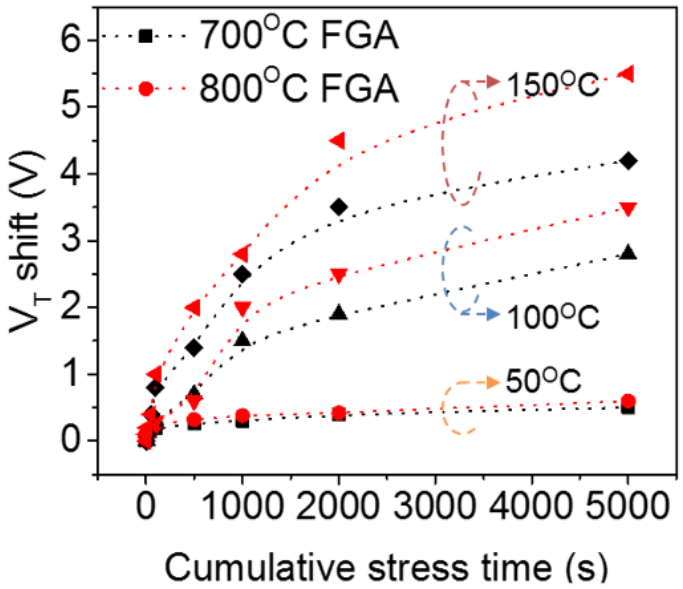
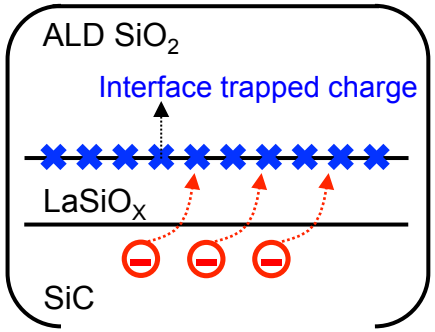
Reliability Results : La_2O_3 varying thickness

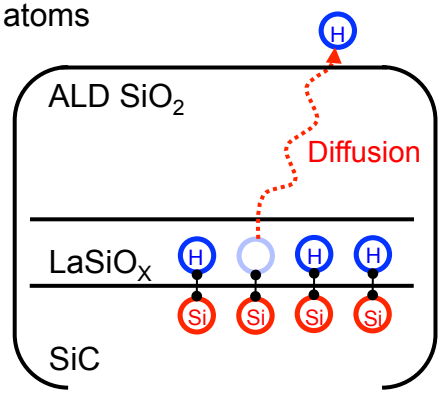
High Temperature Reliability



Case 1. Trapping by ALD SiO_2



Case 2. Out diffusion of hydrogen atoms



- La_2O_3 is known to contain bulk electron traps[1,2]. Electrons in the channel tunnel into the traps.
- Electron trapping in La-silicate[2,3]

- **Larger V_T shift were observed at elevated temperature.**
- **Possible reasons**
  - **Trapping by ALD SiO_2 near the interface**
  - **Access deeper trap at elevated temperature**
  - **Out diffusion of hydrogen atoms**

1. T. Kawanago et al, Microelectronic Engineering, 86, 7–9, 2009, 2. G. Lucovsky et al, J. Vac. Sci. Technol., B22, 2004, 3. N. Inoue et al, Jpn. J. Appl. Phys. 46, 2007.

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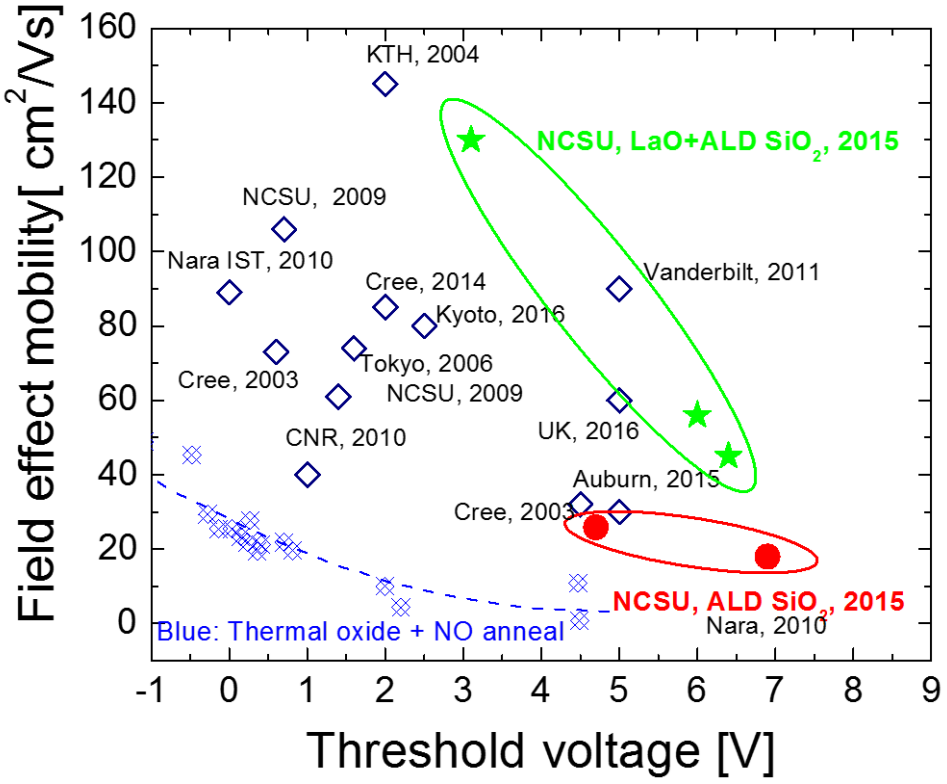
SiC Summary and Future Direction

- **Summary**
  - **Demonstrated 4H SiC lateral MOSFET with V_T > 3V and mobility > 120 cm^2/V-s**
  - **Demonstrated V_T shift < 0.4 V under ± 4MV/cm constant DC stress**
  - **ALD LaO/SiO_2 also confirms high mobility but further optimization is needed.**



Future Plans:

(1) Further reliability study at elevated temperature

(2) Continue on process optimization

(3) Development of Open Process Modules with X-Fab

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Pathway to Market

- Development of standard unit processes typically used in SiC device flows
- Access to foundry with standardized modules
- Development of non-exclusive gate dielectric processes
- Send ALD dielectrics to foundries for evaluation
- Reliability and Cost of new processes
- Need to make sure patent and licensing issues are not barriers
- Commercial grade (wafer size > 6”) ALD tool acquisition will be beneficial for fast adoption of high mobility gate stack.

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Aspirations for PowerAmerica

- How would you like to see the Institute evolve
  - Provide the research community access to manufacturable tools to ensure relevance to foundries
  - Recruit/collaborate with large equipment companies to become part of supply/chain of WBG
  - Use equipment companies to solidify unit processes before transfer to foundries
- Most valuable role the Institute can play
  - Develop a roadmap for SiC devices (like ITRS roadmap for Si)
- What you will do to help the Institute grow
  - Focus on manufacturable SiC devices that provide enhancements in performance and cost and enable PA to gain leadership
  - Support workforce development by training students in WBG research and development
- Unique opportunities/gaps the Institute can exploit
  - Institute should exploit its large expertise of scientists on WBG
  - Institute should come up with a model for sustainability beyond Year 5.

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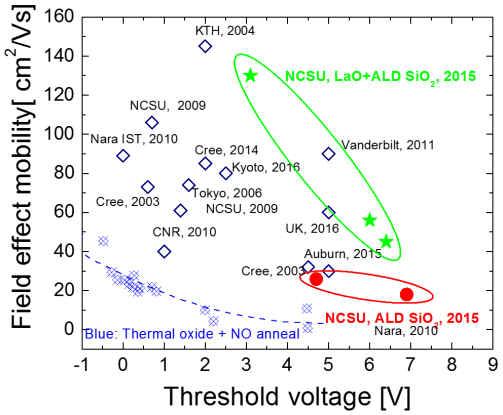
Project Title: **SiC Channel mobility enhancement**

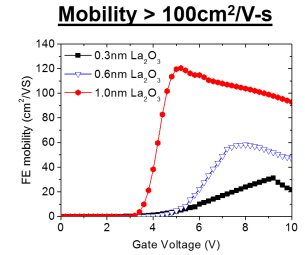
Objectives: **Develop a key module process with foundry, achieve 5X higher mobility, evaluate long term stability, reliability**

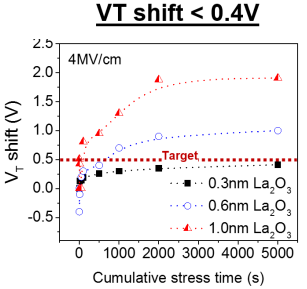
Major Milestones: **Open foundry process & stability / reliability assessment, Optimizing gate stacks for mobility**

Significant Equipment Acquisition:

Deliverables: **SiC device with $\mu > 100cm^2/V{\cdot}s$, $\Delta V_T < \pm 0.4V$ under ±4MV stress and $\Delta V_T < \pm 0.5V$ under ±4MV stress at 150°C**







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WBG Technology Impact

1. WBG SiC and provide high temperature, high voltage, and high speed operation. High mobility SiC and devices will further improve device property while reducing a die size and driver circuits resulting in cost advantages.
2. Medium voltage range applications (~1700V) such as automotive, industrial motors, consumer electronics, PV inverters, etc.
3. Timeframe for commercialization: BP-3
4. Improving SiC mobility by ~50% will reduce on-resistance by ~20% for power devices up to 1700V and result in smaller die size and cost.

More WBG Impact and Additional impacts

1. Our technology can overcome the tradeoff in SiC mobility vs. threshold voltage. With our technology high V_T (3V) is also achieved while maintaining high mobility (>100cm²/V·s).
2. Today, researches of SiC MOSFET reliability raised significant concerns on the long-term operation of SiC MOS-based devices. We are focused on overcoming large threshold voltage shift at elevated temperature.