



Development of an open gate dielectric process for SiC MOSFET manufacturing

SOPO Task #BP2-2.17 CFP28

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Motivation and Objective

- Nitrogen passivation of the interface is the established technology. All methods of inserting nitrogen plateau around the same mobility values
- In this project we are looking beyond Nitrogen using a series of short loop experiments. Lateral MOSFETs of 4 promising technologies are tested:
 - Ultra-High temperature oxidation
 - Ultra-High temperature oxidation with Sb counter doping for higher Field effect mobility
 - Boro-Silicate Glass (BSG) oxide devices
 - Ge strained SiC devices
- The most performant in terms of mobility, stability, oxide strength and compatibility with current fabrication process will be selected for a test run of DMOSFETs

Ultra High Temperature Oxidation

- Easier desorption of the Carbon from the interface

Materials Science Forum Vols. 778-780 (2014) pp 607-610
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doi:10.4028/www.scientific.net/MSF.778-780.607

4H-SiC MOS Capacitors and MOSFET Fabrication with Gate Oxidation at 1400°C

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ELECTRON DEVICES SOCIETY

Received 6 May 2014; revised 6 June 2014; accepted 6 June 2014. Date of publication 8 July 2014; date of current version 21 August 2014. The review of this paper was arranged by Editor M. Chan.
Digital Object Identifier 10.1109/JEDS.2014.2330737

Enhanced Field Effect Mobility on 4H-SiC by Oxidation at 1500°C

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Materials Science Forum Vols. 778-780 (2014) pp 599-602
(2014) Trans Tech Publications, Switzerland
doi:10.4028/www.scientific.net/MSF.778-780.599

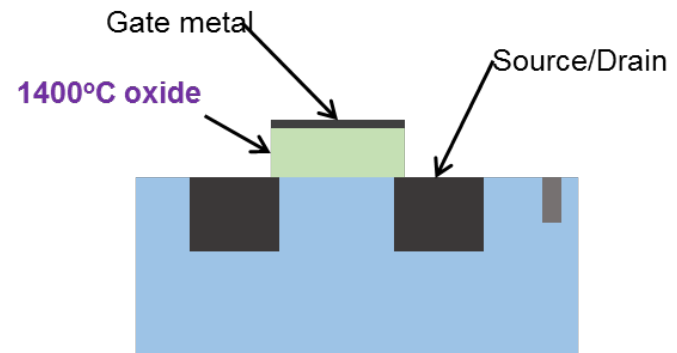
Impact of the oxidation temperature on the interface trap density in 4H-SiC MOS capacitors

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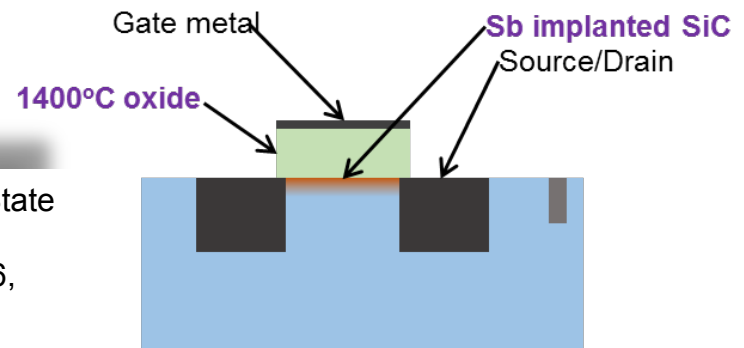
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T. Kobayashi, J. Suda, T. Kimoto, "Reduction of Interface State Density in SiC(0001) MOS structures by Post-Oxidation Ar Annealing at High Temperature," ECSCRM Abstracts, 2016, pp. 203-204.



Ultra high temperature oxidation



Counter doped Ultra high temperature oxide

BSG MOS devices

1176

IEEE ELECTRON DEVICE LETTERS, VOL. 35, NO. 12, DECEMBER 2014

Improved Channel Mobility in 4H-SiC MOSFETs by Boron Passivation

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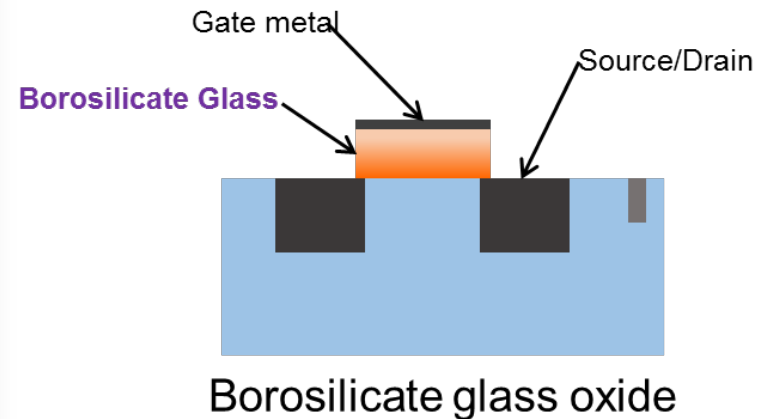
Abstract—We propose another process for fabricating 4H-SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) with high channel mobility. The B atoms were introduced into a SiO₂/4H-SiC interface by thermal annealing with a BN planar diffusion source. The interface state density near the conduction band edge of 4H-SiC was effectively reduced by the B diffusion and the fabricated 4H-SiC MOSFETs showed a peak field-effect mobility of 102 cm²/Vs. The obtained high channel mobility cannot be explained by counter doping because B atoms act as acceptors in 4H-SiC. We suggest that the interfacial structural change of SiO₂ may be responsible for the reduced trap density and enhanced channel mobility.

Index Terms—Boron passivation, channel mobility, interface state density, SiC MOSFETs.

I. INTRODUCTION

Several researchers have suggested that the near-interface traps (NITs) located near the SiO₂/4H-SiC interface may be related to the D_{it} near the conduction band edge of 4H-SiC [4], [10]. Although there have yet to be detailed theoretical and experimental studies on NITs, the removal of interface stress may be effective in reducing NIT density [4], [10]. To reduce interface stress, it may be effective to incorporate network formers such as P₂O₅ into the interface because they reduce the connectivity of the SiO₂ network and thus reduce interface stress [13]. Based on the above considerations, we hypothesize that the incorporation of B may also be effective in reducing the interface stress and thus in reducing the trap density because B₂O₃ is also known to be a network former that reduces the network connectivity of SiO₂ [14].

In this letter, we describe that the channel mobility of



Ge:SiC

APPLIED PHYSICS LETTERS

VOLUME 74, NUMBER 4

25 JANUARY 1

Electrical and optical properties of Ge-implanted 4H-SiC

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APPLIED PHYSICS LETTERS

VOLUME 85, NUMBER 12

20

Pseudomorphic SiC alloys formed by Ge ion implantation

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Influence of 250 keV Ge ions fluence on electrical and optical properties of SiC

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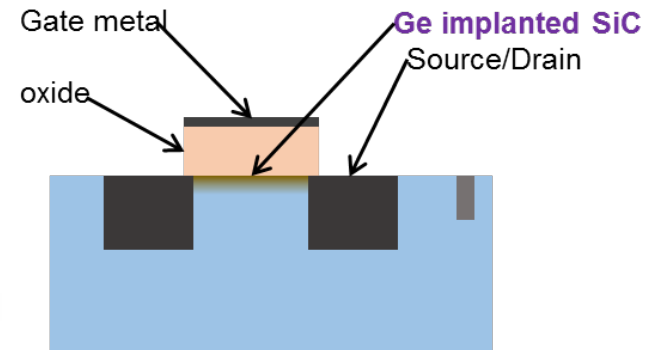
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Received 25 July 2006; received in revised form 10 January 2007; accepted 10 January 2007

Abstract

Commercially graded SiC samples were implanted with 250 keV germanium ions (Ge^+) at room temperature. For Ge^+ ions so laser-induced plasma (LIP) technique was used. Ge^+ implantation was confirmed by energy dispersive X-ray (EDX) analysis. Character FWHM and lattice constant of SiC samples has been observed after the Ge implantation, calculated by Bragg's law from XRD and a comparison of the electrical and optical properties of SiC before and after Ge^+ implantation (SiC:Ge) has also been made. Electrical diagnostic comprises of a four-probe method for the measurement of resistivity whereas Raman spectroscopy is employed for the optical investigation. Resistivity measurements of SiC and SiC:Ge samples showed that resistivity decreases as Ge^+ implantation increases. Raman spectroscopy of the SiC and SiC:Ge showed that Raman band became broadened and is shifted towards the lower wave number with the increase in Ge ion fluence. The increase in Ge ions fluence enhances the lattice defects which are responsible for broadened XRD and Raman peaks as well as increase in conductivity of the samples.

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Ge Strained SiC channel

- Evidence of strain in the SiC lattice
- Lower resistivity

What has been accomplished so far

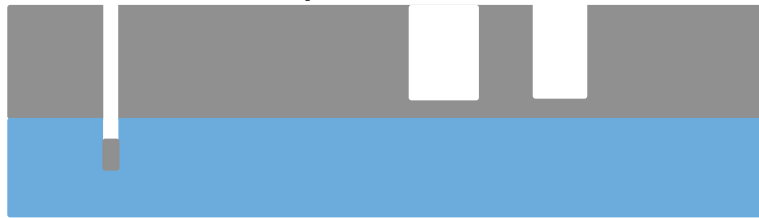
- Fabrication of the of the common template for the devices up to Gate oxide or Gate implant steps.
- Ultra High Temperature Oxide MOS capacitors and MOSFETs
- Borosilicate Glass Devices :
 - Evaluation Borosilicate glass obtained by different methods using MOS capacitors
 - Characterization of BSG MOSFETs from B_2O_3 solid Source

Common Template for all devices

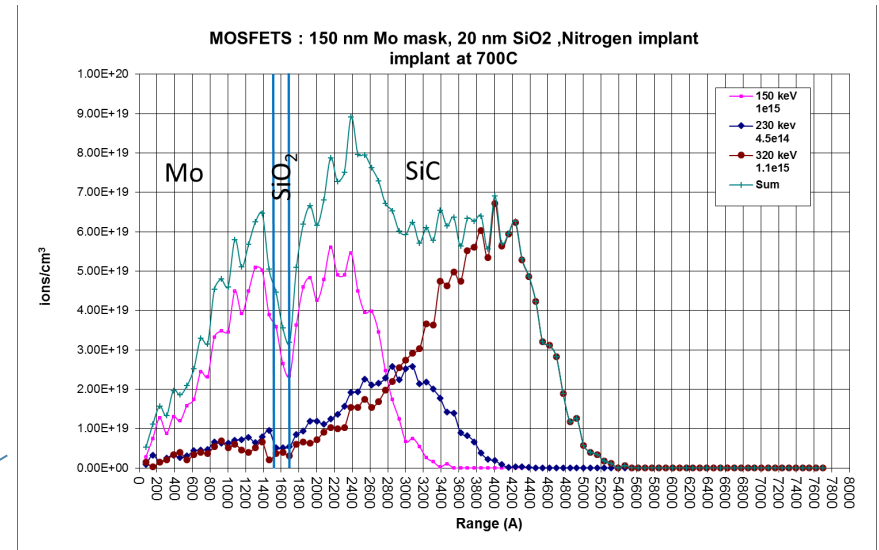
RIE etch



Implant Mask 1

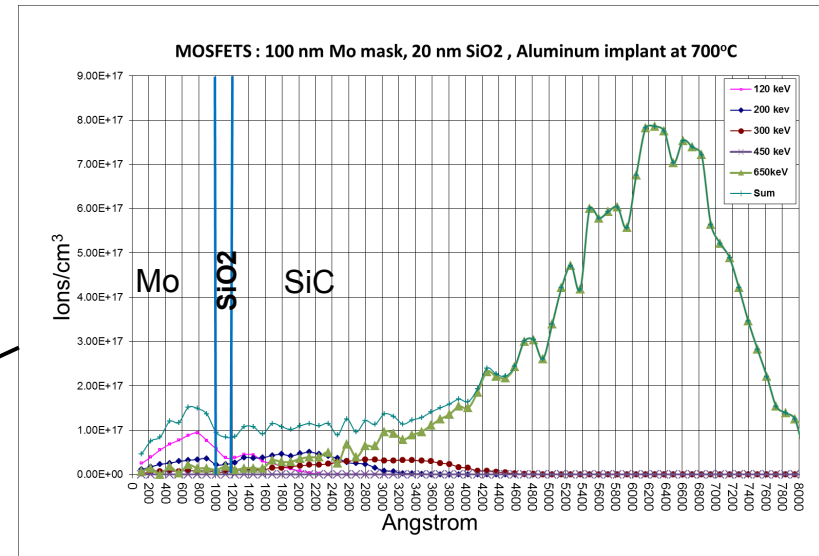
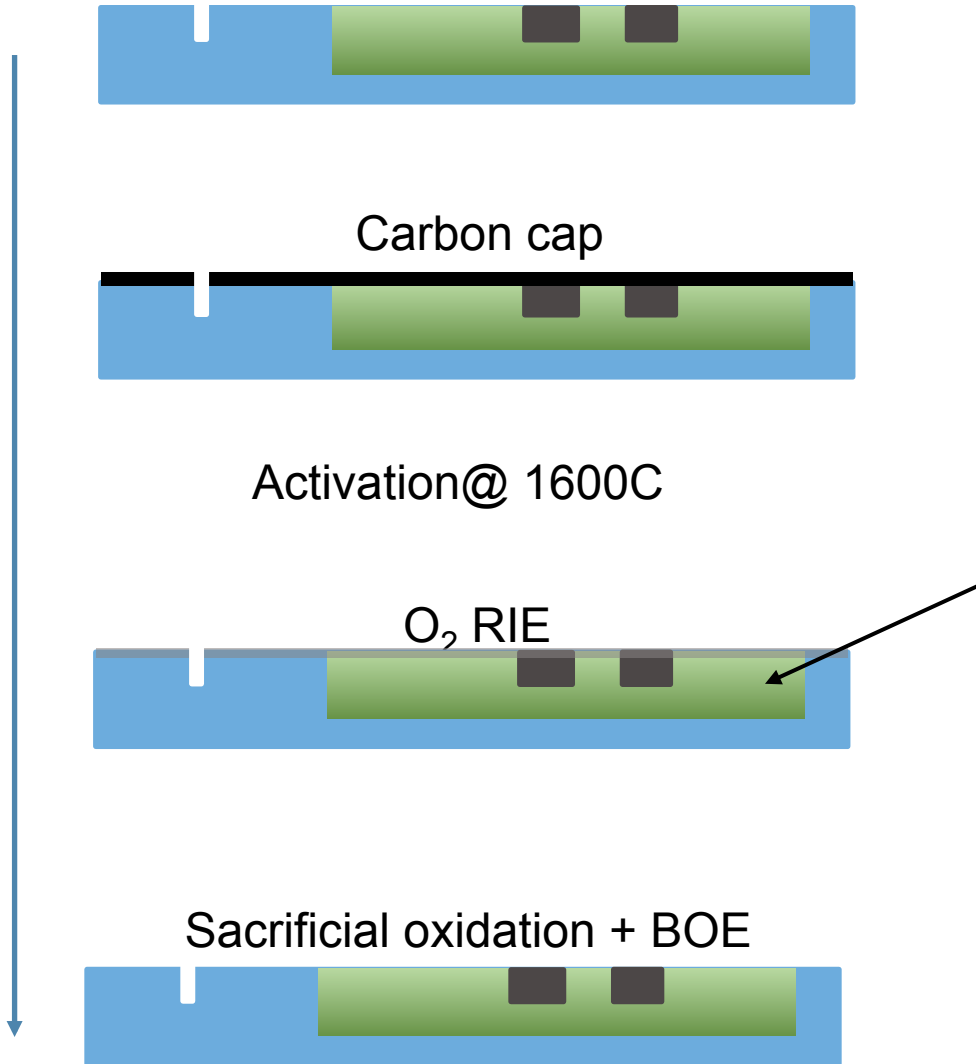


Implant Mask 2



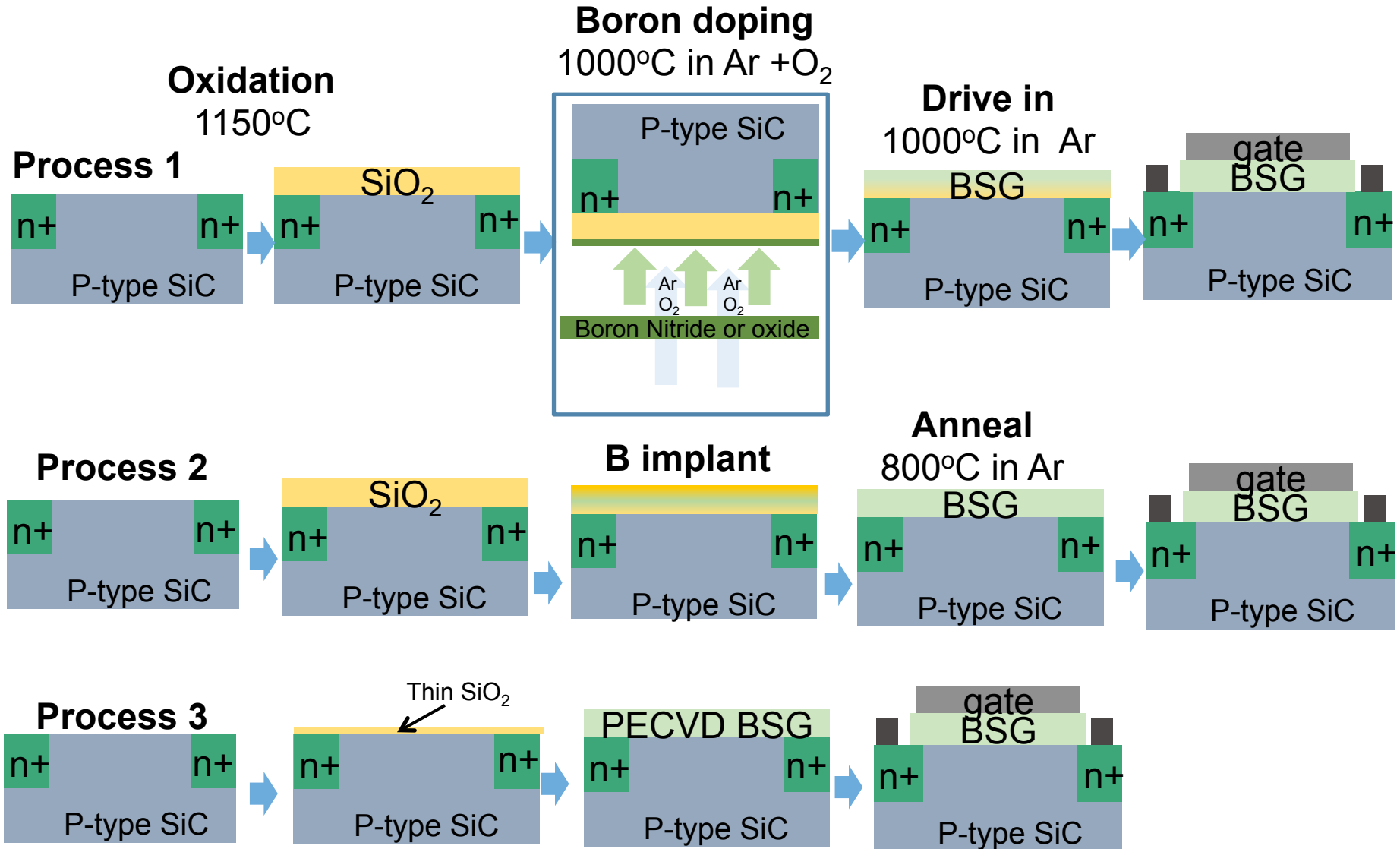
Source/Drain implant

Doping profiles



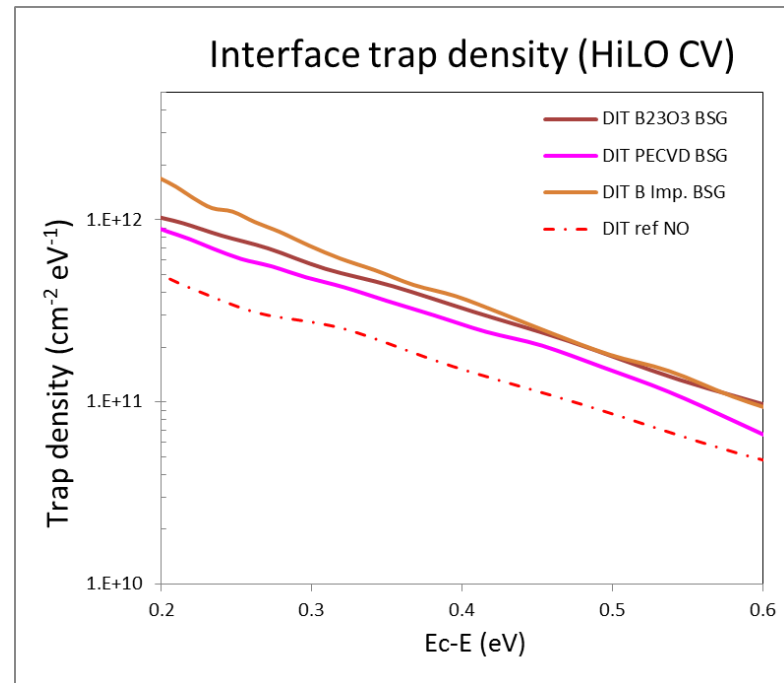
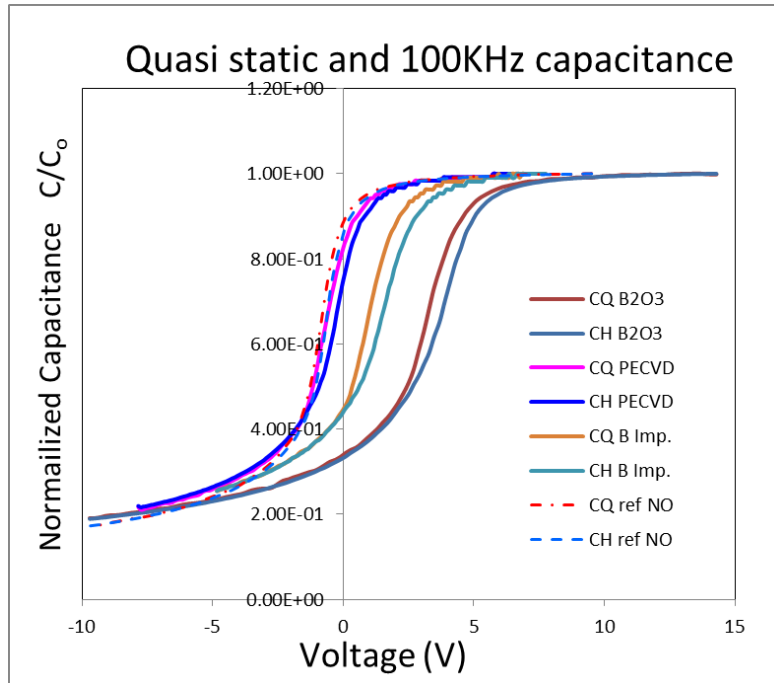
P-well implant

BSG processes



BSG gate oxide devices

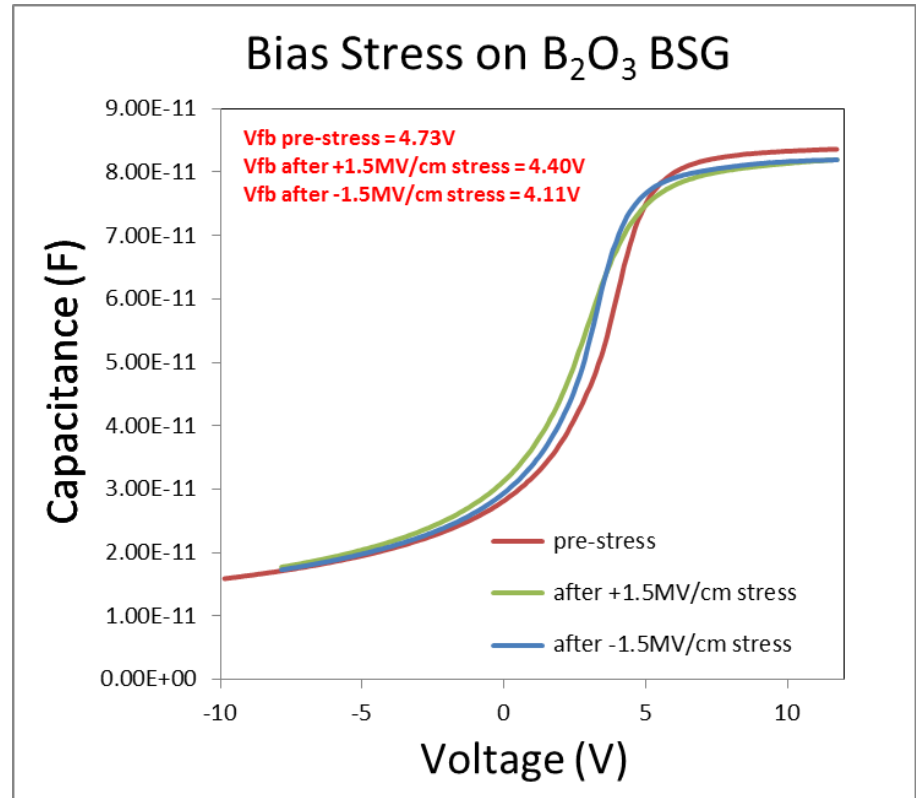
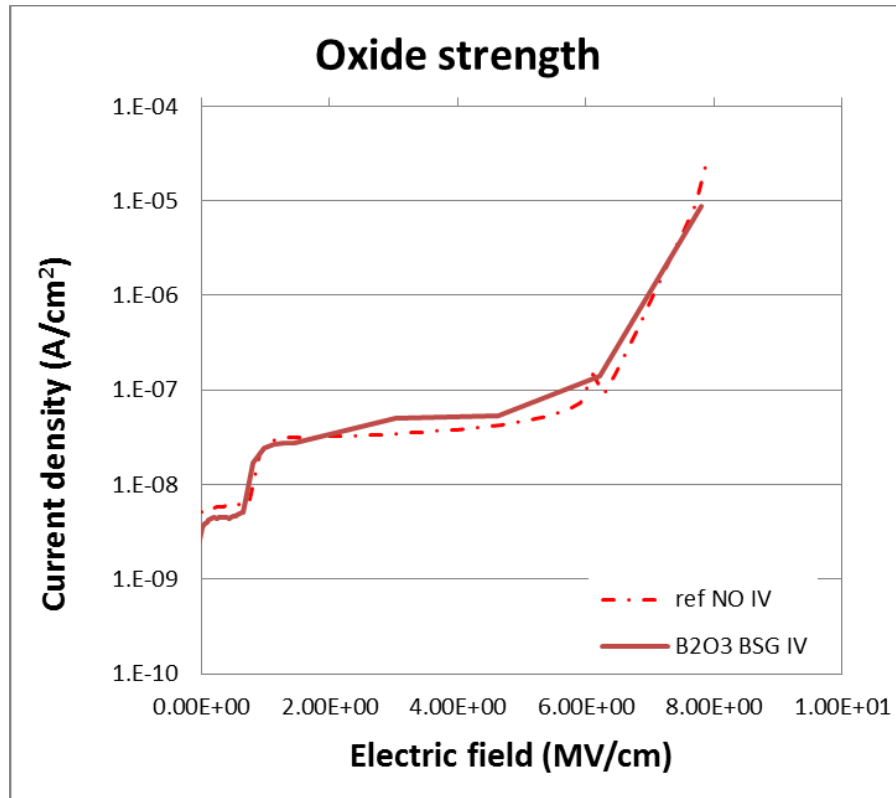
BSG gate oxide devices : comparison of B doping methods



BN solid source doped devices showed too weak oxides to be fully characterized. They have been dropped from the study. The high interface trap density of the implanted Boron devices also shows more in depth work would need to be done on these device. Therefore they were also dropped from this study.

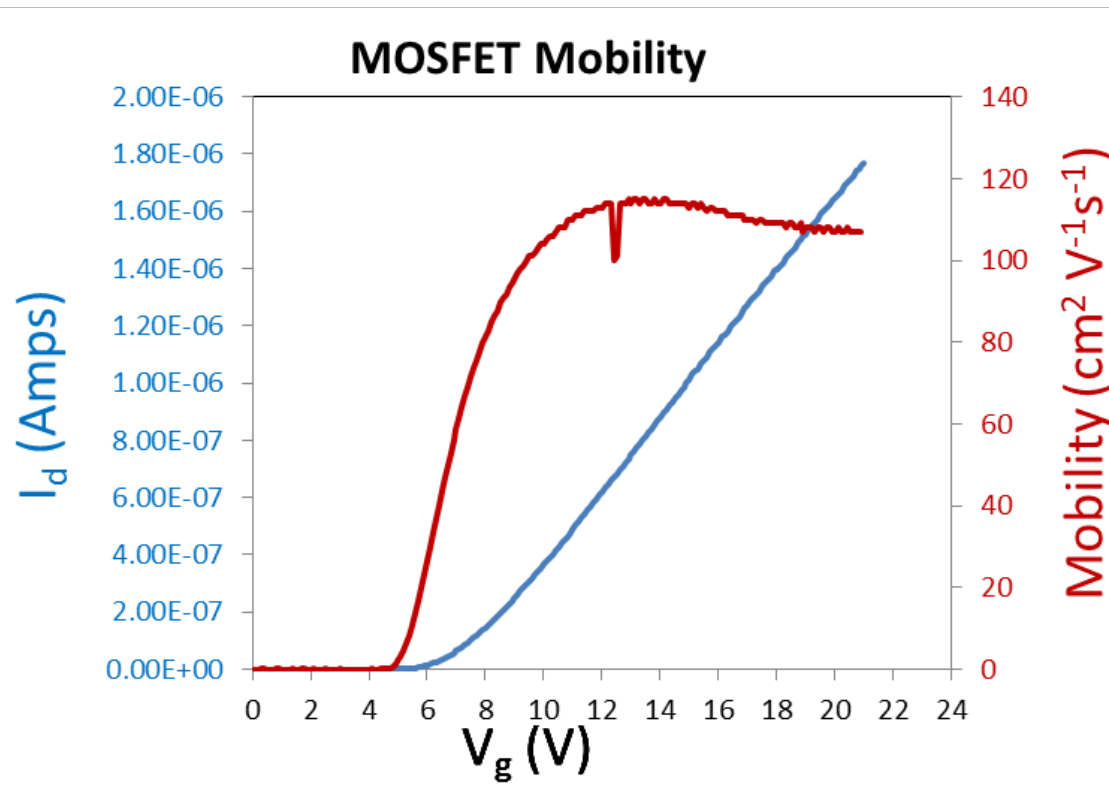
BSG: Oxide strength and stability

BSG gate oxide devices : stability and reliability



Preliminary results have been obtained in oxide breakdown strength and reliability

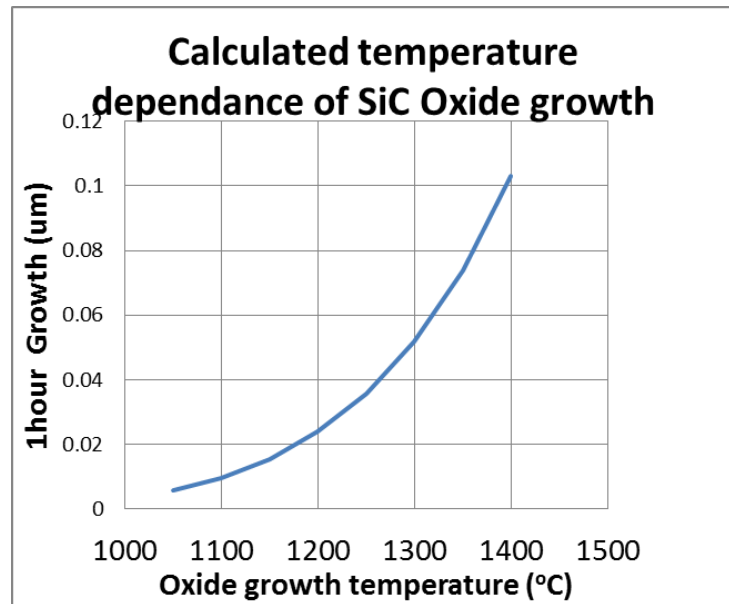
BSG MOSFET (B_2O_3 source)



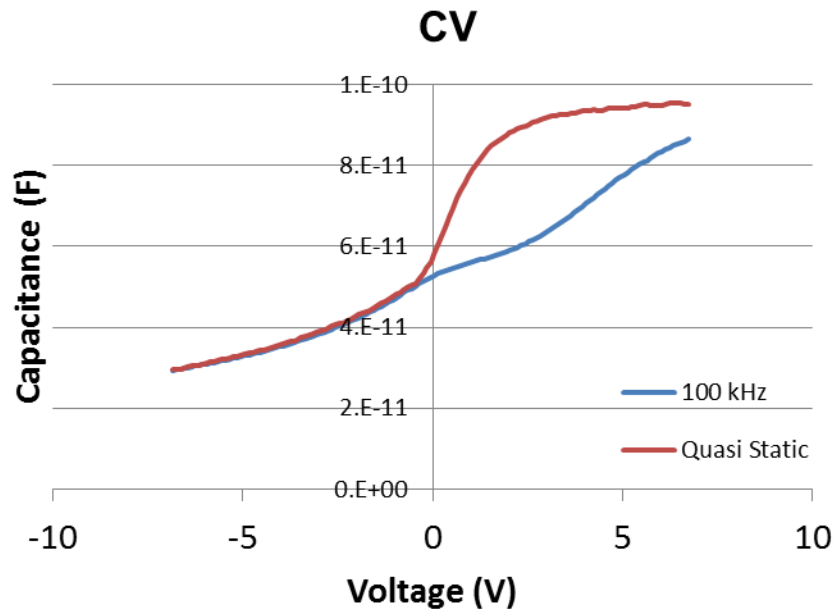
- Devices show high field effect mobility
- Reduced interface trap density
- Residual instability is possibly due to impurity in the doping material
- Deposited BSG shows great promise in reducing unwanted impurities

Ultrahigh temperature Oxidation

- Process 1
 - Oxide growth at 1425°C
 - Ramp up and ramp down under Ar flow
- Process 2
 - Oxide growth at 1150°C
 - Anneal in Ar at 1500°C

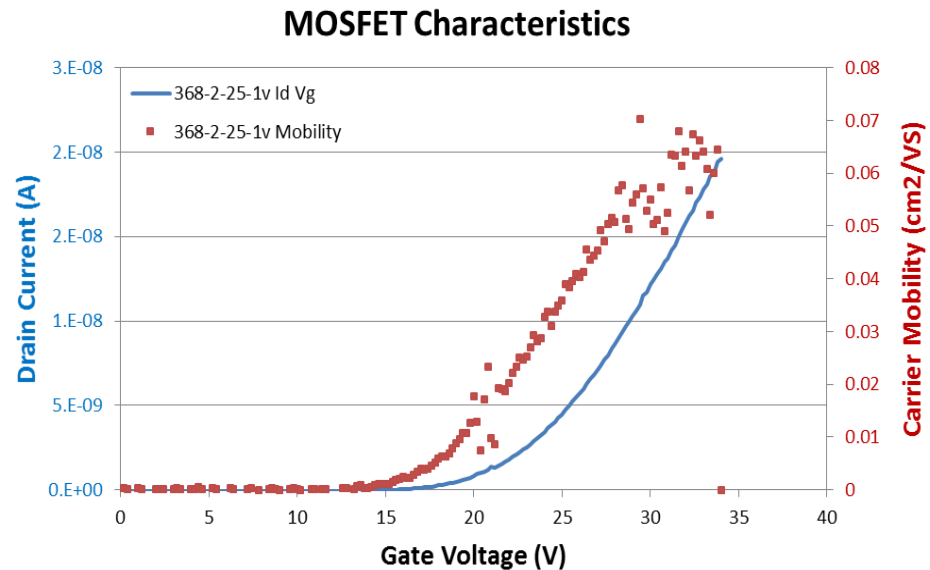


1425°C oxidation

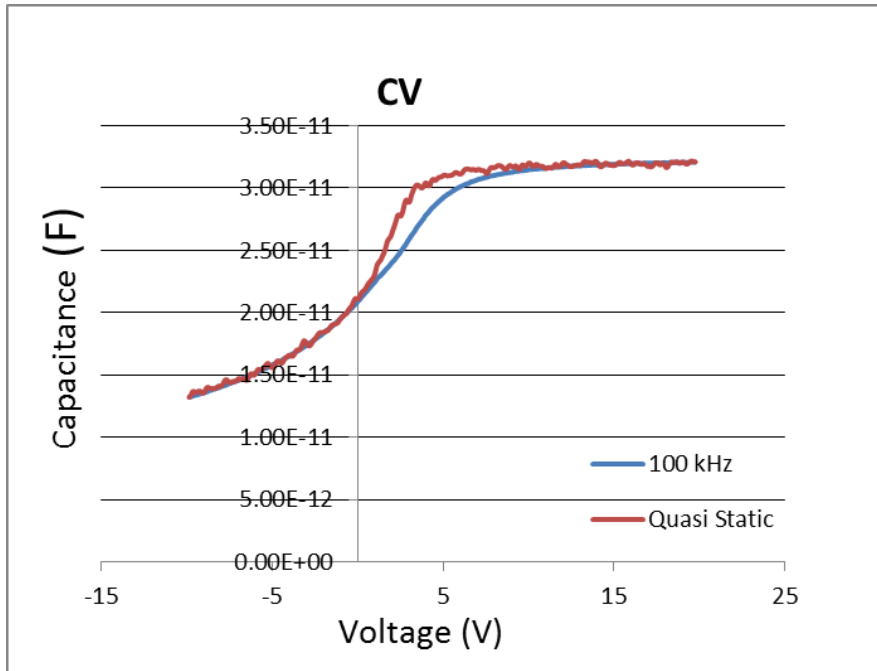


- Low Mobility
- Significant Gate leakage
- High contact resistance due to Al contact

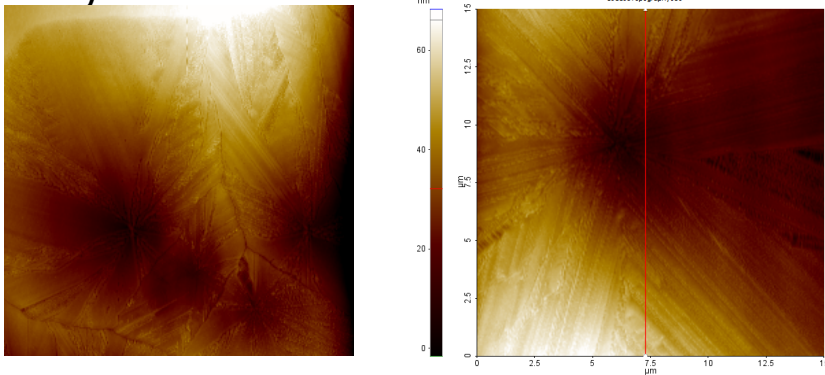
- 10 min in O₂ at 1425°C
- Ramp up and down in Ar
- Thicker than expected oxide, suggests oxidation during ramp up and ramp down
- High trap density; The interface seems unpassivated



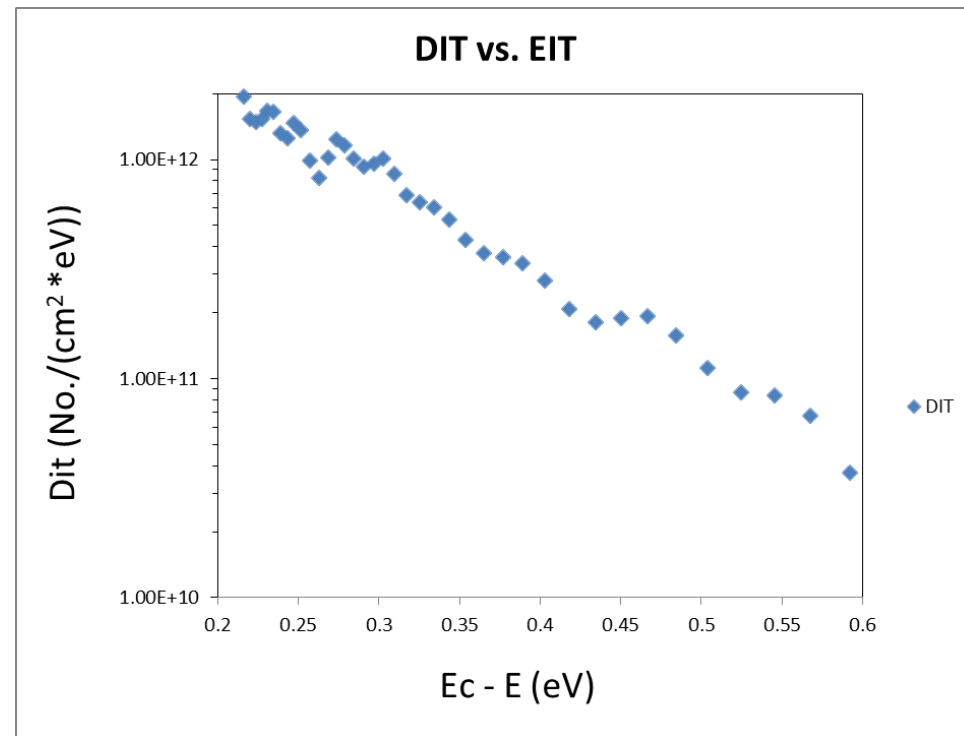
1500°C Ar Anneal



- AFM Image of the oxide shows dendrite-like defects, possibly due to crystallization



- Interface trap density similar to unpassivated oxides
- Original process requires extremely fast cooling that could not be replicated. Ramp down was limited to 5°/min to avoid cracking the furnace tube



Conclusion

- So far Ultra high temperature oxidation did not show any advantage in trap density reduction, oxide strength or carrier mobility.
- A fair evaluation of ultra high temperature oxidation requires process equipment with higher performance to reduce parasitic growth, contamination and cooling rate.
- Devices with Ni ohmic contacts will be made.

Remaining Work

- Sb counter doped Ultra High temperature oxide devices.
- Revisit Ultra High temperature oxide devices with improved set up
- Ge strained SiC devices